In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 12, lines 14 to ~~29~~ 20 as follows:

--The channel request registers pass information used in the source pipeline ~~204~~ 214 for generation of the read/pre-write commands 221. Similarly the channel request registers pass information used in the destination pipeline ~~205~~ 215 for the generation of write ~~command/ write~~ command/write data words 222. Read response data 223 from the ports is returned to the destination pipeline via the data router unit 206.--

A1

Rewrite the paragraph at page 15, lines 1 to 9 as follows:

--Having decided to send a transaction to the port referenced in the P-pipeline stage 405, transfer controller hub 100 sends a decrement signal 401 to the state of master queue counter 251 making ready for the next cycle. This decreases the stored number of available entries in FIFO buffer 410 upon allocation of new data to the port. In this example it is the P-pipeline stage of the next transaction represented by P-pipeline logic 405. This allows multiple transactions to be sent to the same port on consecutive cycles.--

A2

Rewrite the paragraph at page 15, lines 20 to 30 as follows:

--When the port has processed an entry from its queue FIFO buffer 410, it sends a decrement signal 414 to remote queue counter 252 within the port logic. The port logic also sends a confirm decrement signal 408 back to transfer controller hub 100 in the Q-pipeline stage 407. This then sends an increment signal 409 to the master queue counter 251 two cycles later in the P-pipeline stage. The M-pipeline stage 411 is used to map the port state to the associated channels, as ~~its own~~ it owns the channels that transfer

A3

controller hub 100 prioritizes in the P-pipeline stage 405. Thus an emptying of an entry from FIFO buffer 410 means that another entry is available for use.--